CLAIMS

1. An electrically erasable and programmable memory comprising:

a memory array organized in sectors, each sector comprising memory cells linked to bit lines and to word lines, the memory cells linked to a same word line forming one page of the memory array, the memory cells linked to a same bit line being subjected to an electrical stress cycle upon each programming operation of another memory cell linked to the same bit line;

at least one counter for controlling and for refreshing pages of the memory array, comprising data forming tokens usable once before the counter is erased, each token corresponding by its rank in the counter to at least one address of a page to be controlled; and

control and refresh means for managing the counter and arranged for controlling and, if necessary, refreshing pages designated by the counter,

characterized in that:

each sector includes a control and refresh counter that is integrated into the sector and memory cells linked to the bit lines of the sector; and

the control and refresh means are arranged for erasing a counter after reaching a maximum counting value that is chosen so that, when this maximum counting value is reached, memory cells of the counter have undergone a number of electrical stress cycles that is at the most equal to a determined number

2. The memory according to claim 1 wherein the determined number is the maximum number of electrical stress cycles that the pages of the corresponding sector can undergo between two controls.

3. The memory according to claim 1 wherein the maximum counting value of a counter is chosen so that all the pages of the corresponding sector are controlled at least once between two erasures of the counter.

4. The memory according to claim 1 wherein a token designates a determined number of pages, and wherein the maximum counting value of a counter is equal to the maximum number of electrical stress cycles that the pages of the corresponding sector can undergo between two controls, divided by the number of pages that a token designates.

5. The memory according to claim 1 wherein the control and refresh means are arranged for, before or after each programming cycle of a page of a sector, controlling one and only one page of the same sector.

6. The memory according to claim 1, further comprising:

means for allocating to a token of a counter a logic value that is equal to the majority logic value of a group of bits saved in a group of memory cells of the counter, the used or unused state of the token varying according to the majority logic value.

7. The memory according to claim 6 wherein the maximum counting value covers the entire data storage extent offered by the counter, such that each memory cell of a counter receives a bit forming one token part.

8. The memory according to claim 6 wherein a group of memory cells corresponding to one token comprises a number of memory cells equal to the ratio of the number of memory cells of the counter to the number of pages that the sector in which the counter is located comprises.

9. The memory according to claim 1 wherein the control and refresh means are arranged for erasing a counter during the erasure of one page of the sector in which the counter is located.

10. The memory according to claim 1, comprising an address converter for converting the rank of an unused token into the address of a page to be controlled.

11. A method for controlling and for refreshing memory cells in an electrically erasable and programmable memory array organized in sectors, each sector comprising memory cells linked to bit lines and to word lines, the memory cells linked to a same word line forming one page of the memory array, the memory cells linked to a same bit line being subjected to an electrical stress cycle upon each programming operation of another memory cell linked to the same bit line; the method comprising:

controlling and, if necessary, refreshing memory cells of pages of the memory array the address of which is indicated by a control and refresh counter comprising data forming tokens usable once before the counter is erased, each token corresponding, by its rank in the counter, to at least one address of a page to be controlled;

advancing the count on a control and refresh counter that is integrated into each sector of the memory each time memory cells linked to the bit lines of the sector undergo electrical stress cycle, and

erasing a counter of a sector is erased after reaching a maximum counting value that is chosen so that, when this maximum counting value is reached, memory cells of the counter have undergone a number of electrical stress cycles that is at the most equal to a determined number.

12. The method according to claim 11 wherein the determined number is the maximum number of electrical stress cycles that the pages of the corresponding sector can undergo between two controls.

13. The method according to claim 11 wherein the maximum counting value of a counter is chosen so that all the pages of the corresponding sector are controlled at least once between two erasures of the counter.

14. The method according to claim 11 wherein a token designates a determined number of pages, and wherein the maximum counting value of a counter is equal to the maximum number of electrical stress cycles that the pages of the corresponding sector can undergo between two controls, divided by the number of pages that a token designates.

15. The method according to claim 11 wherein a page of a sector is controlled before or after each programming operation of a page of the same sector.

16. The method according to claim 11 wherein the used or unused state of a token of a counter is determined by the majority logic value of a group of bits saved in a group of memory cells of the counter.

17. The method according to claim 11 wherein the maximum counting value of a counter covers all the memory cells of the counter, such that tokens are saved in all the memory cells of the counter.

18. The method according to claim 11, further including:

erasing the counter during the erasure of a page of the sector in which the counter is located.